1) Apparatus for detecting at least one predetermined invalid bit pattern in a digitally encoded bit stream, comprising:

a source of digitally encoded data;

means, responsive to said source, for providing a bit stream having a sequence of at least digitally encoded bit patterns;

said bit patterns having run-length restrictions;

an invalid symbol detector means;

a data bus carrying said digitally encoded bit stream from said source to said invalid symbol detector means; and

said invalid symbol detector means responsive to said bit patterns carried on said data bus for monitoring said bit stream substantially direct from said source of digitally encoded data and for identifying at least one invalid run-length restriction from said digitally encoded bit pattern.

2) Apparatus for detecting at least one predetermined invalid bit pattern in a digitally encoded bit stream as recited in claim 1 and further comprising:

said invalid symbol detector is employed for detecting errors at the run-length bit stream pattern level.

3) Apparatus for detecting at least one predetermined invalid bit pattern in a digitally encoded bit stream as recited in claim 1 and further comprising:

said invalid symbol detector is employed for detecting errors at the symbol level of the bit stream pattern.

4) Apparatus for detecting at least one predetermined bit pattern in a digitally encoded bit stream encoded with channel bit patterns employed to represent original data and the channel bit pattern have run-length restrictions, said apparatus comprising:

a source of digitally encoded data;

means, responsive to said source, for providing a sequence of digitally encoded bit stream patterns having at least channel bit patterns arranged as successive symbols;

said symbols of channel bit patterns having run-length restrictions;

a symbol detector means;

a data bus for carrying said digitally encoded bit stream from said source to said symbol detector means;

said symbol detector means responsive to said data bus for monitoring said bit stream substantially direct from said source of said digitally encoded data and for identifying at least one symbol from said digitally encoded bit pattern.

5) Apparatus for detecting at least one predetermined bit pattern in a digitally encoded bit stream encoded with channel bit patterns employed to represent original data and the channel bit pattern have run-length restrictions as recited in claim 4, said apparatus further comprising:

said symbol detector means reads the data before the data has been de-interleaved.

6) Apparatus for detecting at least one predetermined bit pattern in a digitally encoded bit stream encoded with channel bit patterns employed to represent original data and the channel bit pattern have run-length restrictions as recited in claim 4, said apparatus further comprising:

said symbol detector means reads the data before the data has been placed in ECC blocks.

7) Apparatus for detecting at least one predetermined bit pattern in a digitally encoded bit stream encoded with channel bit patterns employed to represent original data and the channel bit pattern have run-length restrictions as recited in claim 4, said apparatus further comprising:

said symbol detector means reads the data before the data has been processed with traditional error detection and correction circuits.

8) Apparatus for detecting at least one predetermined bit pattern as recited in claim 4 wherein said bit pattern is a valid bit pattern.

9) Apparatus for detecting at least one predetermined bit pattern as recited in claim 4 wherein said bit pattern is an invalid bit pattern.

10) An error mapping control apparatus for a memory array comprising:

a signal source for providing a stream of signals organized into a plurality of localized areas;

a memory array means having a plurality of elements organized for storing error information from a plurality of localized areas from said signal source;

said memory array means having a first input synchronizing signal for resetting said array to a first selected storage position of said memory array;

said first selected position corresponds to said first localized area of said signal source being scanned for errors;

means for identifying said first localized area by its fixed linear distance and fixed radial distance corresponding to said source; and

memory control means for cycling said memory array means through successive array positions corresponding to successive localized areas of said signal source, for summing the errors collected from each of said successive localized area of said source and for storing said summation of said errors in a corresponding one of said elements of said array;

11) An error mapping control apparatus for a memory array as recited in claim 10, wherein each element of said memory array further comprises:

a means for summing errors collected from a localized area defined by a selectable linear distance and a selectable radial distance within said data source.

12) An error mapping control apparatus for a memory array as recited in claim 10, and further comprising:

means for displaying the value in each element in said error map array as a representation of the number of errors associated with each corresponding localized area.

13) An error mapping control apparatus for a memory array as recited in claim 10, wherein said elements of said memory array further comprises:

each of said elements being employed for summing the number of errors found in each of said localized areas; and

the number of elements in the memory array is equal to the number of linear samples in each rotation of the optical media.

14) An error mapping control apparatus for a memory array as recited in claim 13, and further comprising:

means for displaying the value in each element in said error map array as a representation of the number of errors associated with each corresponding localized area.

15) An error mapping control apparatus for a memory array as recited in claim 10, and further comprising:

means for determining the radial resolution of elements of said array by the number of revolutions corresponding to each element.

16) An error mapping control apparatus for a memory array as recited in claim 15, and further comprising:

means for displaying the value in each element in said error map array as a representation of the number of errors associated with each corresponding localized area.

17) An error mapping control apparatus for a memory array as recited in claim 10, and further comprising:

means for incrementing the element value by the detection of an invalid symbol associated with a digital error during the reading of an localized area.

18) An error mapping control apparatus for a memory array as recited in claim 17, and further comprising:

means for displaying the value in each element in said error map array as a representation of the number of errors associated with each corresponding localized area.

19) An error mapping control apparatus for a memory array as recited in claim 10, and further comprising:

means for incrementing the element value by the detection of an invalid run-length associated with a digital error during the reading of an localized area.

20) An error mapping control apparatus for a memory array as recited in claim 19, and further comprising:

means for displaying the value in each element in said error map array as a representation of the number of errors associated with each corresponding localized area.